What is claimed is:

1. A method for analyzing defects in electronic circuit patterns comprising the following steps:

a step for detecting a defect in an inspected object and storing position information for said detected defect;

a step for collecting detailed information of said defect for which said position information is stored and storing said collected detailed information in association with said defect position information;

a step for electronically testing said inspected object and storing position information for a position at which a fault is generated in said electronic test;

a step for comparing said stored defect position information and said fault generating position information;

a step for classifying said detected defect based on results from said comparing step; and

displaying information relating to said classified defect.

2. A method for analyzing defects in electronic circuit patterns as described in claim 1 further comprising a step for selecting a representative sample from said displayed detailed information.

3. A method for analyzing defects in electronic circuit patterns as described in claim 2 further comprising a step for calculating characteristic values from said selected representative samples and determining guidelines for classifying said detailed information based on said calculated characteristic values.

4. A method for analyzing defects in electronic circuit patterns as described in claim 1

further comprising a step for calculating characteristic values from said classified detailed information and generating guidelines for classifying said detailed information based on said characteristic values.

5. A method for analyzing defects in electronic circuit patterns comprising the following steps:

a step for inspecting a first inspected object during a production process and storing information relating to a defect detected by said inspection including position information of said detected defect;

a step for performing an electronic test on said first inspected object after said production process is completed to detect faults in said first inspected object and storing fault generation position information;

a step for comparing said position information of said defect detected in said inspection of said first inspected object during said production process with said electronic test fault generating position detected by said electronic test performed on said first inspected object after said production process is completed;

a step for classifying said detected defect during said production process based on said comparison result; and

a step for outputting information on said classified defect.

6. A method for analyzing defects in electronic circuit patterns as described in claim 5 wherein said detected defect is classified as either a critical defect or a non-critical defect.

7. A method for analyzing defects in electronic circuit patterns as described in claim 6 wherein non-critical defects in said detected defects are further classified into at least two categories.

8. A method for analyzing defects in electronic circuit patterns as described in claim 5 wherein information relating to a fault generation rate for each classification of said classified defects is output.

9. A method for analyzing defects in electronic circuit patterns as described in claim 5 further comprising a step for inspecting a second inspected object during said production process, obtaining information relating to a defect detected in said inspection including position information of said defect, and predicting a critical defect volume for said second inspected object based on said classified defect information and using said information relating to said defect on said second inspected object including said defect position information.

10. A method for analyzing defects in electronic circuit patterns as described in claim 5 wherein a second inspected object is inspected during said production process, information is obtained relating to a defect detected in said inspection including position information of said defect, and a critical defect volume for said production process is predicted based on said information relating to said defect and said classified defect information.

11. A method for analyzing defects in electronic circuit patterns as described in claim 5 wherein a second inspected object is inspected during said production process, information is obtained relating to a defect detected in said inspection including position information of said defect, and a critical defect volume is predicted for each process within said production process based on said information relating to said defect and said classified defect information.

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12. A method for analyzing defects in electronic circuit patterns as described in claim 5 wherein said detected defect images are displayed by classification as said classified defect information.

13. A method for analyzing defects in electronic circuit patterns comprising the following steps:

a step for inspecting a first inspected object during a production process and detecting defects;

a step for obtaining information relating to said detected defects including defect position information;

a step for performing an electronic test on said first inspected object after said production process has been completed and detecting electronic testing faults in said first inspected object;

a step for obtaining information on said detected electronic testing fault generating positions;

a step for comparing said obtained defect position information and said electronic testing fault generating positions and extracting defects for which both position informations match or are close to matching;

a step for classifying said extracted defects into critical defects and non-critical defects and displaying said defects on a screen; and

a step for modifying classifications of said defects displayed on said screen.

14. A method for analyzing defects in electronic circuit patterns as described in claim 13 wherein results of said comparison between said detected defect position information and said electronic testing fault generating positions are output.

15. A method for analyzing defects in electronic circuit patterns as described in claim

13 wherein a second inspected object is inspected during said production process and detected defects are classified using information relating to said information relating to said defect classifications modified on said screen, and a process generating critical defects is determined and/or critical defect generation rates are predicted for each process.

16. A system for analyzing defects in electronic circuit patterns comprising:

a first memory which stores position information of defects detected by a detection of an object;

a second memory which stores detailed information of said defects, which is obtained through an inspection using said position information stored by said first memory means, in association with said position information of said;

a third memory which stores a position information of electrical defects detected by a electrical testing;

a comparater which compares said position information stored in said second memory and said position information of electrical defects stored in said third memory;

a classifying means for classifying said detailed information stored in said second storing means based on comparison results from said comparater; and

an outputting means which output information relating to said detailed information classified by said classifying means.

17. A system for analyzing defects in electronic circuit patterns as described in claim 16 wherein said classifying means calculates characteristic values of said classified detailed information and generates guidelines for classifying said detailed information based on said characteristic values.

18. A system for analyzing defects in electronic circuit patterns as described in claim

16 wherein said detailed information is a defect image and said classifying means classifies said defect images into critical defect images and non-critical defect images.

19. A system for analyzing defects in electronic circuit patterns as described in claim 16 wherein said classifying means classifies said non-critical defect images further into at least two categories.

20. A system for analyzing defects in electronic circuit patterns as described in claim 16 wherein said outputting means outputs information relating to fault generating rates for each classification of said classified defects.

21. A system for analyzing defects in electronic circuit patterns as described in claim 16 wherein said outputting means outputs information relating to critical defect generating volume.

22. A system for analyzing defects in electronic circuit patterns as described in claim 16 wherein said outputting means outputs information relating to a critical defect generating process within said electronic circuit pattern production process.

23. A system for analyzing defects in electronic circuit patterns comprising:

first storing means for storing position information of defects detected through an inspection of a object;

second storing means for storing an image of said defects, which is observed using said position information stored by said first storing means, in association with said position information of said defects;

a third memory which stores a position information of electrical defects detected by a electrical testing;

classifying means for classifying said defect images stored in said second storing means using said defect images stored by said second storing means and electronic test fault generating position information stored by said third storing means; and

outputting means for outputting information relating to said defects classified by said classifying means.

24. A system for analyzing defects in electronic circuit patterns as described in claim 23 wherein said classifying means classifies said defect images into critical defect images and non-critical defect images.

25. A system for analyzing defects in electronic circuit patterns as described in claim 24 wherein said classifying means classifies said non-critical defect images further into at least two categories.

26. A system for analyzing defects in electronic circuit patterns as described in claim 23 wherein said outputting means outputs information relating to fault generating rates for each classification of said classified defects.

27. A system for analyzing defects in electronic circuit patterns as described in claim 23 wherein said outputting means outputs information relating to critical defect generating volume.

28. A system for analyzing defects in electronic circuit patterns as described in claim 23 wherein said outputting means outputs information relating to a critical defect generating process within said electronic circuit pattern production process.